AN ADAPTIVE VOLTAGE SCALING DIGITAL PROCESSING COMPONENT AND METHOD OF OPERATING THE SAME

ABSTRACT OF THE DISCLOSURE

There is disclosed a digital circuit comprising a digital processing component, an adjustable power supply and power supply adjustment circuitry. The digital processing component is capable of operating at a plurality of selected clock frequencies, wherein a maximum delay time of a critical path in the digital processing component is determined by a level of a power supply, VDD, of the digital processing component. The adjustable power supply is capable of supplying VDD to the digital processing component. The power supply adjustment circuitry is operable to receive a first selected clock signal and adjusts the level of VDD such that the maximum delay time of the critical path of the digital processing component is less than a pulse-width duration between a first clock edge of the first selected clock signal and a second clock edge of the first selected clock signal immediately following the first clock edge.